

We Claim:

1. A method for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

providing a nest and a clamping mechanism configured to hold the substrate;

placing the substrate on the nest and aligning the substrate using a plurality of locator pins configured to engage the locator openings;

holding the substrate on the nest using the clamping mechanism;

removing the locator pins from the locator openings;

removing the clamping mechanism;

applying a vacuum to the substrate; and

sawing the substrate held on the nest by the vacuum into separate components.

2. The method of claim 1 wherein the locator pins are mounted to an alignment base configured to hold the nest.

3. The method of claim 1 wherein the locator pins are mounted to the clamping mechanism.

4. The method of claim 1 wherein the locator pins are mounted to a base for holding the nest, and with the nest on the base, the locator pins project through openings in the nest.

5. The method of claim 1 wherein the components comprise an element selected from the group consisting of packages, multi chip modules, printed circuit boards, interconnects, bumped dice and bare dice.

6. The method of claim 1 wherein the substrate comprises a panel and the components are arranged on the panel in at least one row.

5 7. The method of claim 1 wherein the substrate comprises a panel and the components are arranged on the panel in a matrix of rows and columns.

10 8. The method of claim 1 further comprising providing a sawing base configured to hold the base and to apply the vacuum to the substrate during the sawing step.

15 9. A method for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

20 providing a nest configured to hold the substrate;
providing an alignment base comprising a plurality of locator pins configured to engage the locator openings;
placing the substrate on the nest;
25 placing the nest on the alignment base and aligning the substrate on the nest using the locator pins;
providing a sawing base configured to hold the nest and the substrate for sawing;
placing the nest and the substrate on the sawing base;
30 and
sawing the substrate into separate components.

10. The method of claim 9 wherein the sawing base comprises a vacuum opening configured to hold the substrate during the sawing step.

35 11. The method of claim 9 wherein the nest comprises a detachable clamping mechanism which is detached prior to the sawing step.

12. The method of claim 9 wherein the nest comprises a detachable clamping mechanism and at least some of the locator pins are mounted to the clamping mechanism.

13. The method of claim 9 further comprising clamping the substrate to the nest following the placing the nest step, then unclamping the substrate from the nest prior to the sawing step.

14. A method for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

providing an alignment base comprising a plurality of locator pins configured to engage the locator openings;

providing a nest mountable to the alignment base configured to hold the substrate;

aligning the substrate on the nest using the alignment base and the locator pins;

providing a sawing base for holding the nest comprising a vacuum opening configured to hold the substrate on the nest;

mounting the nest to the sawing base with the vacuum opening holding the substrate on the nest; and

sawing the substrate into separate components.

15. The method of claim 14 wherein the substrate comprises a panel, and the components are arranged on the panel in at least one row.

16. The method of claim 14 wherein the substrate comprises a panel, and the components are arranged on the panel in one or more matrix arrays of rows and columns.

17. The method of claim 14 further comprising providing a clamping mechanism configured for attachment to the nest for holding the substrate on the nest, attaching the clamping mechanism to the nest following the aligning step, then
5 removing the clamping mechanism from the nest prior to the sawing step.

18. The method of claim 17 further comprising providing the clamping mechanism with at least some of the locator
10 pins.

19. A method for singulating semiconductor components contained on a substrate:

15 providing the substrate with a plurality of locator openings;

providing a nest configured to hold the substrate comprising a plurality of openings;

providing a clamping mechanism attachable to the nest for clamping the substrate to the nest;

20 providing an alignment base comprising a plurality of locator pins configured to engage the locator openings;

placing the nest on the alignment base with the locator pins projecting from the openings in the nest;

25 placing the substrate on the nest with the locator pins engaging the locator openings;

attaching the clamping mechanism to the nest to clamp the substrate to the nest;

removing the nest from the alignment base;

30 providing a sawing base comprising a vacuum opening configured to apply a vacuum to the substrate held on the nest;

applying the vacuum through the sawing base to the substrate;

removing the clamping mechanism from the nest; and

35 sawing the substrate held on the nest by the vacuum into separate components.

20. The method of claim 19 further comprising providing the clamping mechanism with a plurality of second locator pins configured to engage the locator openings.

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21. The method of claim 19 further comprising providing a saw blade configured to perform the sawing step.

10 22. The method of claim 19 wherein the clamping mechanism comprises latches for engaging the nest, and a compliant pad configured to engage the components.

15 23. The method of claim 19 wherein the nest comprises a plurality of recesses configured to retain the components on the substrate.

20 24. The method of claim 19 wherein the alignment base comprises a plurality of first mounting studs configured to engage a plurality mounting openings on the nest.

25 25. The method of claim 19 wherein the sawing base comprises a plurality of second mounting studs configured to engage the mounting openings on the nest.

26. A system for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

30 a nest configured to hold the substrate;
an alignment base configured to support the nest and to align the substrate on the nest, the alignment base comprising a plurality of locator pins configured with the nest on the alignment base to engage the locator openings to align the substrate on the nest; and

35 a sawing base configured to support the nest and to apply a vacuum to the substrate to hold the substrate on the nest for sawing.

27. The system of claim 26 further comprising a clamping mechanism attachable to the nest configured to clamp the substrate to the nest.

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28. The system of claim 26 wherein the nest comprises a plurality of openings and with the nest on the alignment base the locator pins project from the openings.

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29. The system of claim 26 wherein the alignment base and the sawing base comprise a plurality of mounting studs and the nest comprises a plurality of mounting openings configured to engage the mounting studs.

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30. The system of claim 26 further comprising a clamping mechanism attachable to the nest configured to clamp the substrate to the nest, the clamping mechanism comprising a plurality of second locator pins configured to engage the locator openings.

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31. A system for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

a nest configured to hold the substrate comprising a plurality of openings; and

an alignment base configured to support the nest and to align the substrate on the nest, the alignment base comprising a plurality of locator pins configured with the nest on the alignment base to project from the openings on the nest and to engage the locator openings to align the substrate on the nest.

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32. The system of claim 31 further comprising a sawing base configured to support the nest and to apply a vacuum to the substrate to hold the substrate on the nest for sawing.

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33. The system of claim 31 wherein the sawing base comprises a plurality of pedestals having vacuum openings configured to apply the vacuum to the substrate.

5 34. The system of claim 31 wherein the sawing base comprises a plurality of pedestals having vacuum openings for applying the vacuum and the nest comprises a plurality of pedestal openings for receiving the pedestals.

10 35. The system of claim 31 wherein the substrate comprises a panel with the components thereon in at least one row.

15 36. The system of claim 31 wherein the substrate comprises a panel with the components thereon arranged in one or more matrix arrays.

20 37. The system of claim 31 further comprising a saw blade configured to saw the substrate held on the nest.

38. The system of claim 31 further comprising a clamping mechanism attachable to the nest configured to clamp the substrate on the nest.

25 39. The system of claim 31 further comprising a clamping mechanism attachable to the nest configured to clamp the substrate on the nest, the clamping mechanism comprising a plurality of second locator pins configured to engage the locator openings.

30 40. A system for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

35 a nest configured to hold the substrate comprising a plurality of openings;

a clamping mechanism attachable to the nest for clamping the substrate to the nest;

an alignment base configured to support the nest and to align the substrate on the nest, the alignment base comprising a plurality of locator pins configured to project from the openings in the nest and to engage the locator openings;

a sawing base comprising a vacuum opening configured to apply a vacuum to the substrate held on the nest; and

a saw blade configured to saw the substrate held in the nest on the sawing base.

41. The system of claim 40 wherein the nest comprises a plurality of mounting openings, the alignment base comprises a plurality of first mounting studs for engaging the mounting openings, and the sawing base comprises a plurality of second mounting studs for engaging the mounting openings.

42. The system of claim 40 wherein the clamping mechanism comprises a plurality of second locator pins configured to engage the locator openings on the substrate supported by the alignment base.

43. The system of claim 40 wherein the alignment base comprises a plurality of recesses for retaining the components.

44. The system of claim 40 wherein the sawing base comprises at least one pedestal for supporting the components and the vacuum opening is located in the pedestal.

45. The system of claim 40 wherein the clamping mechanism comprises at least one latch and the nest comprises at least one slot for engaging the latch.

46. The system of claim 40 wherein the components comprise an element selected from the group consisting of packages, multi chip modules, printed circuit boards, interconnects, bumped dice and bare dice.

47. The system of claim 40 wherein the substrate comprises a panel and the components comprise packages on the panel.

48. The system of claim 40 wherein the substrate comprises a panel and the components comprise packages arranged on the panel in one or more matrix arrays.

49. A system for singulating semiconductor components contained on a substrate having a plurality of locator openings comprising:

a nest configured to hold the substrate;

a clamping mechanism attachable to the nest for clamping the substrate to the nest, the mechanism comprising a plurality of locator pins configured to engage the locator openings to align the substrate on the nest; and

a sawing base comprising a vacuum opening configured to apply a vacuum to the substrate held on the nest.

50. The system of claim 49 further comprising an alignment base configured to support the nest with the clamping mechanism attached thereto, the alignment base comprising a plurality of second locator pins configured to engage the locator openings to align the substrate on the nest.

51. The system of claim 49 wherein the nest comprises a plurality of opening for receiving the locator pins.

52. The system of claim 49 wherein the nest comprises a plurality of mounting openings and the sawing base comprises

a plurality of mounting studs for engaging the mounting openings.

53. A system for singulating semiconductor components
5 contained on a substrate having a plurality of locator openings comprising:

a nest configured to hold the substrate comprising a plurality of openings aligned with the locator openings, a plurality of recesses configured to retain the components and
10 a plurality of pedestal openings;

an alignment base configured to support the nest and to align the substrate on the nest, the alignment base comprising a plurality of locator pins configured with the nest on the alignment base to project from the openings on
15 the nest and to engage the locator openings to align the substrate on the nest; and

a sawing base configured to support the nest and the substrate thereon for sawing, the sawing base comprising a plurality of pedestals configured to project from the
20 pedestal openings and vacuum openings in the pedestals configured to apply a vacuum to the components.

54. The system of claim 53 further comprising a clamping mechanism attachable to the nest for clamping the
25 substrate on the nest.

55. The system of claim 54 wherein the clamping mechanism comprises a plurality of second locator pins configured with the nest on the alignment base to engage the
30 locator openings.